Cont A1

45. (New) The method according to claim 44, wherein the one of the cover substrate and the cover layer includes contact springs for contacting electric terminals of the electronic components.

46. (New) The method according to claim 45, wherein the contact springs are produced by a galvanic deposition of metal.

REMARKS

This Preliminary Amendment cancels without prejudice original claims 1 to 23 and claims 1 to 21 in the annex to the International Preliminary Examination Report, in the underlying PCT Application No. PCT/DE99/03469, and adds without prejudice new claims 22 to 46. The new claims conform the claims to U.S. Patent and Trademark Office rules and do not add new matter to the application.

In accordance with 37 C.F.R. § 1.121(b)(3), the Substitute Specification (including the Abstract, but without the claims) contains no new matter. The amendments reflected in the Substitute Specification (including Abstract) are to conform the Specification and Abstract to U.S. Patent and Trademark Office rules or to correct informalities. As required by 37 C.F.R. § 1.121(b)(3)(iii) and § 1.125(b)(2), a Marked Up Version Of The Substitute Specification comparing the Specification of record and the Substitute Specification also accompanies this Preliminary Amendment. Approval and entry of the Substitute Specification (including Abstract) is respectfully requested.

The underlying PCT Application No. PCT/DE99/03469 includes an International Search Report, dated March 13, 2000. The Search Report includes a list of documents that were uncovered in the underlying PCT Application. A copy of the Search Report accompanies this Preliminary Amendment.

The underlying PCT application also includes an International Preliminary Examination Report, dated April 3, 2001, and an annex. An English translation of the International Preliminary Examination Report and the annex accompanies this Preliminary Amendment.

Applicants asserts that the subject matter of the present application is new, non-obvious, and useful. Prompt consideration and allowance of the application are respectfully requested.

Respectfully Submitted,

Dated: 6/7/01

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METHOD OF PACKAGING ELECTRONIC COMPONENTS

Field Of The Invention

The present invention relates to a method of packaging electronic components such as Gunn diodes.

Background Information

For an anti-collision radar system in a motor vehicle (ACC = adaptive cruise control), radar waves at frequencies above 50 gigahertz are used. Gunn diodes made of a III-V semiconductor material such as GaAs or InP are used to produce these radar waves[; when]. When a d.c. voltage is applied, [they] these diode elements generate a high frequency electromagnetic wave. The Gunn diode element has a diameter of 70 µm and a thickness of 10 µm, for example, and is contacted on its top and bottom sides.

Such known Gunn diodes are usually completely encased and hermetically sealed in a package composed of a bottom part, a ceramic ring, and a cover part. The ceramic ring functions as an insulator between the two poles of the diode and also absorbs mechanical contact forces and installation forces in use of the diode. A bonded gold foil ("Maltese cross") is used for contacting the diode. Such a package must be manufactured in sequential process steps and is therefore expensive. Owing to tolerances in the manufacturing processes and components, a relatively great scattering in the high frequency properties of the packaged component is unavoidable.

[Advantages of the] Summary Of The Invention

The method of packaging electronic components [defined by Claim 1] according to the present invention includes the steps of producing a plurality of cavities on a package substrate, mounting the electronic components in the cavities, sealing the cavities with a cover layer or a cover substrate and insulating the components packaged in this way. With the method according to the present invention, a large number of component packages can be manufactured at the same time in one operation, which greatly reduces the manufacturing costs.

The package substrate may be made of a semiconductor material such as silicon or a photopatternable glass. This has the advantage that the technology of processing of silicon or photopatternable glass can be controlled very well and therefore very low manufacturing tolerances can be achieved. This makes it possible to achieve a very good reproducibility of the high frequency properties.

The method according to the present invention also makes it possible to produce packages having very small dimensions and a low stress level due to differences in thermal expansion of different materials.

Silicon, glass or glass ceramic material is also capable of reliably absorbing mechanical contact forces and installation forces which occur during use.

On its side facing away from the cover substrate or cover layer, the package substrate may be provided with a metal layer which is responsible for contacting the packaged electronic component. If the package substrate is made of a semiconductor material, then the side of the package substrate facing the cover substrate or the cover layer is advantageously provided with an insulation layer to insulate

the two poles of the electronic component.

The cavities in the package substrate may be designed in the form of through holes or merely as shallow cavities in the package substrate surface.

In an advantageous refinement of the method according to the present invention, the electronic components to be packaged are arranged on a component carrier layer in a number corresponding to the number of cavities produced in the package substrate, the step of mounting the electronic components in the cavities being accomplished by joining the package substrate and the component carrier layer. The latter may be designed as a metal, in particular as a silver layer.

The cover layer may be made of a semiconductor material such as silicon. The cover layer which is optionally used as an alternative may be made of an organic dielectric into which contact holes are introduced. If the cover substrate is made of a conducting material, the component may be contacted to advantage by a microstructured contact spring mounted on the side of the cover substrate facing the cavity. This ensures permanent and reliable contacting of the component.

If the cover layer is made of an organic dielectric, the side of the component facing upward may be contacted to advantage by means of a metal layer which is vapor deposited or sputtered in a contact hole in the organic dielectric. A photosensitive paint such as a polyimide or BCB (benzocyclobutene) is therefore especially suitable as the organic dielectric.

The packaged electronic components can then be separated by a sawing operation and are then available for further processing on a sheet called a "blue tape."

According to another advantageous variant of this method, insulator structures which function as side walls of the package are arranged outside the package substrate, which is made, for example, of a photosensitive glass; these structures correspond to the known ceramic ring. However, these insulator structures may also be produced simultaneously in large numbers corresponding to the number of components to be packaged, and thus inexpensively, e.g., by selective etching of the photopatternable glass.

To fabricate the component package, the cover substrate is first joined to the package substrate, and then the component carrier layer together with the components is placed on it[, or conversely]. Conversely, the component carrier layer may be joined first to the package substrate and then the cover substrate placed on top.

[Figures] Brief Description Of The Drawings

[Additional advantages of the present invention are explained in greater detail below on the basis of the description with reference to the accompanying drawings, which show:]

Figure 1 shows a schematic diagram [to illustrate] illustrating the method according to the present invention[;].

Figure 2 [:] shows a schematic diagram [to illustrate] illustrating a variant of the method according to the present invention[;].

Figure 3 [:] shows a component package produced by the method according to the present invention, having a deep cavity and a microstructured contact spring[;].

Figure 4 [:] shows a component package having a deep cavity and a cover layer produced from an organic dielectric, the

component package being produced by the method according to the present invention[;].

Figure 5 [:] shows a component package having a shallow cavity and an organic dielectric as the cover layer, the component package having been produced by the method according to the present invention[;].

Figure 6 [:] shows a component package produced by the method according to the present invention having a flat cavity and a cover layer made of an organic dielectric with additional rear-side contacting[;].

Figure 7 [:] shows the essential process steps of an embodiment of the method according to the present invention[;].

Figure 8 [:] shows the essential process steps of another embodiment of the method according to the present invention.

[Embodiments] Detailed Description

To illustrate the method according to the present invention for packaging an electronic component, Figure 1 shows package substrate 2, which has already been provided with cavities 6 to accommodate electric components 8, e.g., Gunn diodes, and a cover substrate 4. Package substrate 2 may be formed by an Si wafer, for example, but other materials such as photopatternable glass are also possible. A regular two-dimensional arrangement of cavities 6 is produced in the silicon surface by a photolithographic method and subsequent etching steps or by essentially known micromechanical structuring methods. The size of the cavities depends on the size of the component to be packaged or any contact springs or the like. In the example illustrated in Figure 1, the depth of the cavities amounts to approximately one-third of the

thickness of package substrate 2. However, the depth of the cavity may also be less. On the other hand, it is also possible to design the cavity as a through hole in the package substrate, as illustrated in Figures 2 [through], 3 and 4 or Figure 7, for example.

For contacting a contact arranged on the underside of component 8, which is already present in the cavity on the left, package 2 may be provided with a conductive layer 3 on its underside, the current flowing through the silicon package substrate from conductive layer 3 to the underside of electric component 8. For insulation with respect to cover substrate 4 by means of which a contact on the top side of the component is contacted to advantage, an insulating layer 5 made of silicon dioxide or silicon nitride, for example, is provided on the top side of package substrate 2. This layer is preferably applied before etching of cavities 6.

After preparing cavities 6, they are fitted with components 8, whereupon the package is closed by applying cover substrate 4, which may also be made of silicon. For contacting a contact arranged on the top side of the component, i.e., diode 8, a contact spring, which is preferably produced by galvanic deposition on cover substrate 4, is used, as shown in Figure 3, for example, where it is labeled with reference number 9. After positioning and gluing cover substrate 4 on package substrate 2, the individually packaged diodes can be separated by sawing, for example, and then are available for further processing. In comparison with the traditional method, where each package is manufactured individually by the methods of precision mechanics, simultaneous production of a large number of packages greatly reduces costs. Since the silicon etching technique permits a high precision, the individual component packages can be manufactured with a high accuracy, so this yields a good reproducibility of the high frequency properties which depend on the dimensions. The low manufacturing

tolerances also permit very small dimensions of the package in an advantageous manner, so that the mechanical stresses during operation, due to differences in thermal expansion of different materials used in the package, remain low.

It should be pointed out that insulation layer 5 shown in Figure 1 can be omitted if package substrate 2 is made of an insulating material such as photosensitive glass. It is then of course impossible to contact the diode via the substrate material.

Figure 2 illustrates a variant of the method according to the present invention for packaging electronic components. Package substrate 2, a silicon wafer or a glass wafer, is thinned in the central area where it is provided with openings. The remaining thick substrate edge stabilizes the substrate and can be used for handling purposes. Through holes 6 form the cavities to receive the electronic components. Insulation material 7, e.g., SiN or SiO_2, is applied to the walls of the through holes as shown in Figure 7. In contrast with the process variant illustrated with reference to Figure 1, components 8 in the method illustrated in Figure 2 are arranged on a component carrier layer 16, e.g., a GaAs wafer. Wafer 6, which forms the component carrier layer, preferably has a smaller diameter than Si wafer 2, which forms the package substrate, so that it finds space in the central area of the wafer which has been etched thin. Components 8 are preferably produced in a joint process on component carrier layer 16. This operation of mounting components 8 in cavities 6 then takes place by joining component carrier wafer 16 to substrate wafer 2. This variant simplifies the assembly operation, permitting even less expensive production method on the whole.

Figure 3 shows a cross-sectional view of a first embodiment of a component package manufactured by the method according to

the present invention. A cavity 6 is produced by micromechanical etching in package substrate 2 made of silicon. A component 8 such as a Gunn diode is arranged in cavity 6, its upper contact being contacted by a contact spring 9 produced micromechanically by galvanic deposition of metal. Cover substrate 4 is also made of a semiconductor material such as silicon and is used to supply electric power to the upper diode contact. The lower diode contact is contacted by a conductive layer 3 made of metal, for example, applied to the lower side of the substrate by vapor deposition or sputtering. An insulating layer 5 is provided for insulation of the two poles.

Figure 4 illustrates another embodiment of a component package produced by the method according to the present invention before separation. As in the case of the embodiment illustrated in Figure 3, a deep cavity 6 has been etched in package substrate 2 and fitted with component 8. In the embodiment illustrated in Figure 4, cover layer 4 is formed by an organic dielectric such as a photosensitive lacquer, for example. An etched pit is formed in this layer, by which a contact layer 11 of vapor deposited or sputtered metal establishes contact with the top side of the diode.

Another embodiment of a component package produced by the method according to the present invention is shown in Figure 5 before separation. In contrast with the embodiment illustrated in Figures 3 and 4, the cavity 6 here is designed only as a shallow cavity. Component 8 is contacted from beneath by the conductive substrate itself, while the electric connection to the top side of the component is accomplished by a contact layer [6] 13 formed in a recess in an organic dielectric which functions as cover layer 4, as in the embodiment illustrated in Figure 4.

In the additional embodiment of a component package produced

by the method according to the present invention and illustrated in Figure 6, package substrate 2 is made of a material having little or no conductivity, such as photopatternable glass, so that no contact layer 15 for contacting the front side of the diode facing downward is necessary. This layer is applied to package substrate 2 by sputtering or vapor deposition after etching a contact hole.

Figure 7 shows schematically the process steps of an embodiment of the method according to the present invention. Figure 7a illustrates one component 8 on a component carrier layer 16 as representative of a plurality of components on component carrier layer 16. In the embodiment according to the present invention illustrated here, component carrier layer 16 is made of silver, for example. Package substrate 2 in which cavities 6 designed as passages have already been prepared by etching is positioned above it, insulation material 7 made of SiN or SiO_2, for example, being applied to the edges of the passages.

Figure 7b illustrates the condition in the production process after joining the package substrate to component carrier layer 16. Then cover layer 4 made of an organic photosensitive dielectric such as BCB is applied (Figure 7c) before component carrier layer 16 is removed by an etching operation or the like and the remaining arrangement is cured by heating, for example (Figure 7d).

Then contact holes are produced in the organic dielectric at the position of the respective components (Figure 7e), e.g., by a photostructuring method or laser machining method, optionally removing the dielectric between the packages.

Figure 7f illustrates the condition when a contact layer for contacting component 8 has been sputtered through the contact hole. Then the individually housed components are separated by

sawing or the like (Figure 7g).

Figure 8 illustrates schematically another embodiment of the packaging method according to the present invention. In contrast with the methods described with reference to Figures 1 through 7, package substrate 20 here is designed as a carrier layer formed from insulator structures 21 which correspond to the ceramic rings of the related art. Carrier layer 20 is made of a photopatternable glass which is available under the brand name Foturan®, for example. Figures 8a through 8d at the left illustrate this carrier layer 20 in cross section and at the right, photomask 18 as seen from above. As shown in Figure 8a, carrier layer 20 is first exposed through mask 18 in the areas indicated with dotted lines and is tempered. This defines the areas of glass to be etched later. Then a metal plating is applied to both sides and metal plating 22 on the front side is structured (Figure 8b). There thus remain circular unplated areas on the top side of glass wafer 20 through which circular holes 23 are etched in glass wafer 20, as indicated schematically in Figure 8c. Then the metal plating is removed from the rear side (Figure 8d). Next, carrier layer 20 structured in this way is joined to a carrier layer 4 provided with a sacrificial layer 4a. Microstructured contact springs 9 are applied to the inside of carrier layer 4. In the process step illustrated in Figure 8f, the areas of glass exposed in process step 8a are etched away, so that only ring-shaped insulator structures made of glass remain of the carrier layer, corresponding to ceramic rings 32 in the related art. Then a component carrier layer 16 having components 8 is joined to it as illustrated in Figure 2, forming closed cavities 6 having components 8 and contact springs 9 inside them. Next, sacrificial layer 4a is etched away (Figure 8g). Finally, the components produced in this way and packaged are separated by sawing, for example, and then are available for further processing. An enlarged view of a finished packaged component is illustrated in Figure 8i.

The method according to the present invention permits simultaneous production of a large number of packages for electronic components, including contacting, with a high precision and low manufacturing costs.

Abstract Of The Disclosure

A method of packaging electronic components includes the steps of forming a plurality of cavities [(6)] in a package substrate [(2; 20),] mounting the electronic components [(8)] in the cavities[(6)], sealing the cavities [(6)] with a cover substrate or a cover layer [(4)] and separating the components [(8)] packaged in this way. This permits inexpensive simultaneous production of a plurality of component packages. In one variant of the method, the components are arranged on a component carrier layer[(16)], the components being mounted in the cavities [(6)] by joining the package substrate [(2; 20)] and the component carrier layer[(16)].

[Figures 1 and 2]